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GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
SPITTLE, MATTHEW D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,017	ONER, KORAY	
	Examiner	Art Unit	
	MATTHEW D. SPITTLE	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 20 have been examined.

Claim Objections

Claim 8 is objected to because of the following informalities: Claim 8 contains the phrase, "…couples the merged interrupt value for **the** each data channel…". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (5,905,897) in view of Moyer et al. (U.S. 6,449,675).

Regarding claim 1, Chou et al. teach an apparatus comprising:

An interrupt indication register associated with each data channel for storing a merged interrupt value representing at least one interrupt source for the associated data channel, where each interrupt indication register is combined to form a merged interrupt status register (Fig. 6, Fig. 9, 41);

An interrupt mapping register associated with each data channel for storing a processor identification for each associated data channel (Fig. 5, 32);

For each data channel, a demultiplexing circuit (Fig. 9, 72 and 74) associated with the data channel for coupling the merged interrupt value for each data channel to a processor identified by the processor identification (col. 8, line 40 – col. 9, line 14).

Chou et al. fail to teach interrupt status registers.

Moyer et al. teach a similar data processing system having interrupt circuitry with a first interrupt status register (Fig. 2, 51) for storing at least one interrupt source (Fig. 2, 42) for a first data channel;

and a second interrupt status register (Fig. 2, 52) for storing at least one interrupt source (Fig. 2, 43) for a second data channel;

and an interrupt indication register (Fig. 2, 59, 60) associated with each data channel for storing a merged interrupt value representing said at least one interrupt source for the associated data channel, where each interrupt indication register is combined to form a merged interrupt status register (Fig. 2, 58).

Moyer et al. teaches this circuitry for providing an interrupt pending signal (Fig. 2, 92), which is needed in the system of Chou et al. (see Fig. 6, signals ipr[0] req - ipr[15] req.; Note that the interrupt pending register (58) of Moyer corresponds to the interrupt

pending register of Chou et al. (41)) for the purpose of providing a simple hardware assist mechanism that can improve the performance of software interrupt handling schemes while requiring minimal circuitry (col. 1, lines 60 – 67).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the circuitry of Moyer et al. into the interrupt system of Chou et al. for the purpose of providing an interrupt pending signal from a series of interrupt sources. This would have been obvious in order to improve the performance of the system. Additionally, known work in one field of endeavor may prompt variations of it for use in the same field (interrupt handling) based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art.

Regarding claim 2, the additional limitation of wherein the apparatus of claim 1 is formed in a packet manager input circuit for mapping a plurality of input sources from a plurality of input channels such that the first data channel comprises a first input channel and the second data channel comprises a second input channel; the Examiner notes that this limitation recites differences that are found only in the labeling of the structures taught by Chou et al. and Moyer et al. These labels are not functionally related to the structure of the prior art. Thus, this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see *In re Gulack*, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); *In re Lowry*, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

Regarding claim 3, the additional limitation of wherein the apparatus of claim 1 is formed in a packet manager output circuit wherein the first data channel comprises a first output virtual channel and the second data channel comprises a second output virtual channel; the Examiner notes that this limitation recites differences that are found only in the labeling of the structures taught by Chou et al. and Moyer et al. These labels are not functionally related to the structure of the prior art. Thus, this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see *In re Gulack*, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); *In re Lowry*, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

Regarding claim 4, Moyer et al. teach the additional limitation wherein the plurality of data channels comprises at least one input channel having a first plurality of interrupt sources (Fig. 2, 42) and at least one output channel having a second plurality of interrupt sources (Fig. 2, 43) and wherein the merged interrupt status register comprises a first interrupt indication register (Fig. 2, 59) associated with said at least one input channel for storing a merged interrupt value representing the first plurality of interrupt sources and a second interrupt indication register (Fig. 2, 60) associated with said at least one output channel for storing a merged interrupt value representing the second plurality of interrupt sources.

Regarding claim 5, Moyer et al. teach the additional limitation of a first mask register (Fig. 2, 55) for selectively masking the at least one interrupt source for the first data channel, wherein the merged interrupt value comprises a masked merged interrupt value.

Regarding claim 6, Moyer et al. teach the additional limitation wherein the first mask register is programmable to select which interrupt source is masked (col. 3, lines 29 – 33).

Regarding claim 7, Chou et al. teach the additional limitation wherein the processor identified by the processor identification determines an interrupting channel by running an interrupt service routine that first reads the merged interrupt status register to identify which data channel generated the interrupt and then reads the interrupt status register corresponding to the identified data channel to determine the interrupt source for the interrupt channel (col. 4, lines 48 – 62).

Regarding claim 8, Chou et al. teach the additional limitation wherein each interrupt mapping register further comprises a priority level indication (Fig. 9, 36) associated with each channel for prioritizing any interrupt issued by the data channel, whereby the demultiplexing circuit selectively couples the merged interrupt value for the each data channel to a plurality of prioritized processor interrupt signals (Fig. 9, 72)

under control of the processor identification and priority level indication (Fig. 10, Fig. 11).

* * *

Claims 9 – 11, 13, and 16 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (5,905,897) in view of Moyer et al. (U.S. 6,449,675).

Regarding claim 9, Chou et al. teach an interrupt mapper comprising:

A channel register that stores the interrupt indication values for the plurality of channels (Fig. 6, Fig. 9, 41);

A plurality of processor map storage devices, each processor map storage device storing a processor identification value for one of the plurality of channels (Fig. 5, 32);

A demultiplexer for mapping each interrupt indication value for a channel to a processing core identified by the processor identification for that channel (Fig. 9, 72 and 74; col. 8, line 40 – col. 9, line 14).

Chou et al. fail to teach source registers, a mask register, and a channel merge circuit.

Moyer et al. teach a similar data processing system having interrupt circuitry with a plurality of source registers (Fig. 2, 51, 52) where each source register identifies interrupt sources (Fig. 2, 42, 43) for one of the plurality of channels;

A mask register (Fig 2, 55) associated with each of the plurality of source registers for selectively masking said associated source register to generate masked interrupt sources for each channel;

A channel merge circuit for merging the masked interrupt sources for each channel into an interrupt indication value for said channel (Fig. 2, 70, 71);

A channel register that stores the interrupt indication values for the plurality of channels (Fig. 2, 58)

Moyer et al. teaches this circuitry for providing an interrupt pending signal (Fig. 2, 92), which is needed in the system of Chou et al. (see Fig. 6, signals ipr[0] req - ipr[15] req.; Note that the interrupt pending register (58) of Moyer corresponds to the itnerrupt pending register of Chou et al. (41)) for the purpose of providing a simple hardware assist mechanism that can improve the performance of software interrupt handling schemes while requiring minimal circuitry (col. 1, lines 60 – 67).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the circuitry of Moyer et al. into the interrupt system of Chou et al. for the purpose of providing an interrupt pending signal from a series of interrupt sources. This would have been obvious in order to improve the performance of the system. Additionally, known work in one field of endeavor may prompt variations of it for use in the same field (interrupt handling) based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art.

Regarding claim 10, Moyer et al. teach the additional limitation of a plurality of AND gates coupled to the source registers and mask registers for generating the masked interrupt sources for each channel (Fig. 2, 70, 71, 72, 73, 74).

Regarding claim 11, Chou et al. teach the additional limitation wherein each processor map storage device stores a processor identification value and a priority level for one of the plurality of channels (Fig. 9, 36, 32).

Regarding claim 13, Moyer et al. teach the additional limitation wherein a processing core that receives an interrupt reads the channel register to determine which channel generated the interrupt and then reads the plurality of source registers to determine a source for the channel's interrupt (col. 3, lines 16 – 18; col. 6, lines 22 – 43).

Regarding claim 16, Moyer et al. teach the additional limitation wherein interrupts from each channel are mapped to only one processing core (Fig. 1, 12).

Regarding claim 17, Chou et al. teach the additional limitation of the plurality of processor map storage devices are programmable to dynamically assign channel interrupts to the processing system cores to implement load balancing among the processing cores (col. 9, lines 3 – 49).

Claims 18 – 20 are directed to claims having substantially similar limitations as in claims 9 – 11, 13, 16 and 17 above, and are therefore rejected under the same rationale.

* * *

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (5,905,897) in view of Moyer et al. (U.S. 6,449,675) and what is old and well known in the art as evidenced by Feldbaumer et al. (U.S. 5,586,046) and Fletcher et al. (U.S. 5,155,387).

Regarding claim 12, Moyer et al. teach AND gates implementing the channel merge circuit, but fail to teach OR gates.

The Examiner takes Official Notice that it was well known in the art at the time of invention by Applicant to interchange AND and OR gates, depending upon system requirements, through the use of DeMorgan's theorum. This is evidenced by Feldbaumer et al. (col. 4, lines 50 – 57), and Fletcher et al. (col. 9, lines 25 – 28).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to substitute OR gate circuitry for the AND gate circuitry in the system of Moyer et al. since to do so was routine in the art.

* * *

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (5,905,897) in view of Moyer et al. (U.S. 6,449,675) and Park (U.S. 5,903,779).

Regarding claim 14, Chou et al. and Moyer et al. fail to teach wherein the plurality of source registers and the channel register are each sized to match a processing width of the processing core.

Park teaches that when the register size is not equivalent to the processor word size, it takes multiple access cycles to transfer data (col. 1, lines 25 - 36).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to size the source registers and channel register to match the processing width of the processing core in order for data transfers to only require a single access cycle. This would have been obvious in order to optimize data transfers, and thus improve the performance of the system as a whole.

Regarding claim 15, Moyer et al. teach the additional limitation wherein the processing core determines the source of an interrupt with two register reads (col. 6, lines 22 – 43).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW D. SPITTLE whose telephone number is (571)272-2467. The examiner can normally be reached on Monday - Friday, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. D. S./
Examiner, Art Unit 2111

/MARK RINEHART/
Supervisory Patent Examiner, Art Unit 2111